

# Defect And Fault Tolerance In VLSI Systems: Volume 2

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## **Yield and reliability of vlsi circuits**

List of Yield and Reliability Related Circuits," Defect and Fault Tolerance in VLSI Systems, Vol. 2, on Defect and Fault Tolerance in VLSI Systems,

## **Dblp: defect and fault tolerance in vlsi systems**

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Publication Title Volume Issue Start Page. Search Basic Search; 20th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems

### **Defect and fault tolerance in vlsi systems -**

Defect and Fault Tolerance in VLSI Systems Volume 1. Authors: Koren, Israel

### **Proceedings 2001 ieee international symposium on**

photocopy beyond the limits of US copyright law, for private use of patrons, those articles in this volume Defect and Fault Tolerance in VLSI Systems, 2001.

### **And fault tolerance in vlsi systems ( dft'06)**

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An Interactive Yield Estimator as a VLSI CAD tool 168 International Workshop on Defect and Fault Tolerance in VLSI Systems D(T) vol. 35, no. 2,

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Defect and Fault Tolerance in VLSI Systems: Volume 1 Israel Koren in Books, Magazines, Textbooks | eBay

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### **Marco [defect and fault tolerance group ]**

Marco Ottavi is currently an Associate Professor at the University of Rome Tor Vergata , before he was a Research Professor with the same University as the

### **Dft abbreviation stands for defect and fault**

Defect and Fault Tolerance definition, categories, type and other relevant information provided by All Acronyms. DFT stands for Defect and Fault Tolerance

### **Ieee xplore abstract - defect and fault tolerance**

The homogeneous structure of field programmable gate arrays (FPGAs) suggests that the defect tolerance can be achieved by shifting the configuration data inside the FPGA.

### **Defect and fault tolerance in vlsi systems, 1998**

Defect and Fault Tolerance in VLSI Systems, 1998. Proceedings., 1998 IEEE International Symposium on. This volume covers topics including:

### **Defect and fault tolerance (article, 2008)**

Get this from a library! Defect and fault tolerance. [Nur A Touba; A Salsano; M Choi;]

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BibTeX @MISC{Andr s\_combineddefect, author = {David De Andr s and Juan-carlos Ruiz and Daniel Gil and Pedro Gil}, title = {Combined Defect and Fault Tolerance for

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### **Gabriele saucier (editor of defect and fault**

Gabriele Saucier is the author of Logic And Architecture Synthesis Fast Prototyping Of Vlsi: Defect and Fault Tolerance in VLSI Systems: Volume 2 by C H

### **Defect and fault tolerance in vlsi systems:**

Defect and Fault Tolerance in VLSI Systems: Volume 2: C.H. Stapper, V.K. Jain, Gabriele Saucier: 9780306435317: Books - Amazon.ca

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Defect and Fault Tolerance in VLSI Systems. Volume 1. Israel Koren . Broschiertes Buch Sprache: Englisch

### **Analysis of fault tolerance in artificial neural**

Proc. 1990 International Workshop on Defect and Fault Tolerance in VLSI Systems, Grenoble, France, Nov. 1990. June 1994, Vol. 1, pp. 333 338.

### **Ieee xplore - conference table of contents**

Publication Title Volume 1998. Proceedings., 1998 IEEE International Proceedings 1998 IEEE International Symposium on Defect and Fault Tolerance in VLSI

### **Defect and fault tolerance in vlsi [and**

Bibliographic content of Defect and Fault Tolerance in VLSI [and Nanotechnology] Systems

### **1997 workshop on defect and fault-tolerance in**

Title: DFT '97 1997 Workshop on Defect and Fault-Tolerance in VLSI Systems table of contents:

Publisher: IEEE Computer Society Washington, DC, USA

### **Dft - defect and fault tolerance in vlsi systems**

Defect and Fault Tolerance in VLSI Systems. Publications: 1070 | Citations: 4659. Fields of study:

Hardware & Architecture

### **Tnano special issue - defect and fault tolerance -**

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### **Citeseerx citation query an interactive yield**

An interactive yield estimator as a VLSI CAD tool," in IEEE Int. Workshop on Defect and Fault Tolerance in VLSI vstems (1993)

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